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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,970	ALSUP ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Fritz M. Fleming

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
AU 2181
7/7/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-41 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 04/27/2006.

Withdrawn Objections

3. Applicant, via amendment, has overcome the objections to claims 37 and 38 set forth in the previous Office Action. Consequently, these objections have been withdrawn by the examiner.

Withdrawn Rejections

4. Applicant, via amendment and argument, has overcome the 35 U.S.C. § 112, first paragraph, rejection of claim 10 set forth in the previous Office Action. Consequently, this rejection has been withdrawn by the examiner.

Maintained Rejections

5. Applicant has failed to overcome the 35 U.S.C. 102 and 35 U.S.C. 103 rejections set forth in the previous Office Action for claims 1-41. Therefore, these rejections are respectfully maintained by the examiner and copied below for applicant's convenience.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 1, 15-17, 27-29, 39, and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Tran, U.S. Patent No. 5,864,689. In addition, "Intel Architecture Software Developer's Manual – Volume 1: Basic Architecture" (Herein referred to as Manual) is cited as extrinsic evidence for showing the operation of x86 CALL and RETURN instructions.

8. Referring to claim 1, Tran has taught a microprocessor, comprising:

a dispatch unit *(microcode unit and instruction decode unit; Fig. 1, components 45 and 36)* configured to dispatch operations *(column 4, lines 29-41; column 6, lines 17-46)*;

a scheduler *(reservation station)* coupled to the dispatch unit and configured to schedule dispatched operations for execution *(column 6, lines 51-63)*;

wherein in response to receiving a microcoded instruction, the dispatch unit is configured to dispatch to the scheduler a microcode subroutine call operation that includes a tag *(target address)* identifying a microcode subroutine associated with the microcoded instruction *(column 8, line 55 – column 9, line 4) [The execution of the x86 CALL instruction involves the storing of context information (such as the instruction pointer) in addition to the execution of the routine (microcode subroutine instructions in*

the context of Tran) [See definition of x86 CALL instruction on page 4-5 in Manual]. In order for context information to be stored, the x86 CALL instruction itself must be executed by one of the execution units of the processor. Execution by one of the execution units requires that the instruction be dispatched from decode unit (part of the dispatch unit) to the reservation station (i.e. the scheduler) associated with the desired execution unit].

9. Referring to claim 15, Tran has taught the microprocessor of claim 1, wherein a same opcode is used to specify the microcode subroutine call operation and a non-microcode subroutine call operation *(column 4, lines 42-54)*.

10. Referring to claim 16, Tran has taught the microprocessor of claim 1, wherein the microcode subroutine includes a return operation, wherein the return operation pops a return address from the stack, wherein execution of the microcode subroutine call operation pushes the return address onto the stack *(column 4, lines 42-54)*.

11. Referring to claim 17, Tran has taught a computer system, comprising:

A system memory *(main memory; Fig. 16, component 16)*; and

A microprocessor *(microprocessor; Fig. 5, component 12)* coupled to the system memory; wherein the microprocessor comprises:

a dispatch unit *(microcode unit and instruction decode unit; Fig. 1, components 45 and 36)* configured to dispatch operations *(column 4, lines 29-41; column 6, lines 17-46)*;

a scheduler *(reservation station)* coupled to the dispatch unit and configured to schedule dispatched operations for execution *(column 6, lines 51-63)*;

wherein in response to receiving a microcoded instruction, the dispatch unit is configured to dispatch to the scheduler a microcode subroutine call operation that includes a tag *(target address)* identifying a microcode subroutine associated with the microcoded instruction *(column 8, line 55 – column 9, line 4)*.

12. Referring to claim 27, given the similarities between claim 15 and claim 27 the arguments as stated for the rejection of claim 15 also apply to claim 27.

13. Referring to claim 28, given the similarities between claim 16 and claim 28 the arguments as stated for the rejection of claim 16 also apply to claim 28.

14. Referring to claim 29, Tran has taught a method comprising:

receiving a stream of instructions *(column 6, lines 13-16)*;

detecting a microcoded instruction within the stream of instructions, wherein the microcoded instruction immediately precedes an other instruction in program order *(column 4, lines 36-41)*;

in response to said detecting, dispatching a microcode subroutine call operation that identifies a microcode subroutine associated with the microcoded instruction *(column 8, line 55 – column 9, line 4)* , wherein the microcode subroutine call operation pushes an address of the other instruction onto a stack *(x86 Call instruction - column 4, lines 42-54)*; and

executing a plurality of operations included in the microcode subroutine, wherein the plurality of operations include a return operation, and wherein execution of the return operation pops the address from the stack *(x86 Return instruction - column 4, lines 42-54)*.

15. Referring to claim 39, given the similarities between claim 15 and claim 39 the arguments as stated for the rejection of claim 15 also apply to claim 39.

16. Referring to claim 41, Tran has taught a system comprising:

Means for receiving a stream of instructions, decoding each non-microcoded instruction within the stream of instruction into one or more operations, and dispatching each of the one or more operations *(decode unit; column 6, lines 17-28)*;

Means for executing dispatched operations *(execution unit; column 6, lines 32-43)*;

Wherein the means for receiving the stream of instructions are configured to detect a microcoded instruction within the stream of instruction and to responsively dispatch a microcode subroutine call operation that identifies a microcoded subroutine associated with microcoded instruction *(column 8, line 55 – column 9, line 4)*;

Wherein the means for executing dispatched operations are configured to push an address onto a stack when executing the microcode subroutine call operation (x86 Call instruction), wherein the address identifies an operation generated by decoding a non-microcoded instruction immediately subsequent to the microcoded instruction within the stream of instructions *(column 4, lines 42-54)*.

17. Claim 40 is rejected under 35 U.S.C. 102(b) as being anticipated by Carbine et al., U.S. Patent No. 5,630,083 (Herein Referred to as Carbine).

18. Referring to claim 40, Carbine has taught a method comprising:

Dispatching one or more operations included in a first microcode subroutine and one or more operations included in a second microcode subroutine *(executing a first and second generic microcode routine; column 12, lines 36-56)*, wherein said dispatching the one or more operations in the first microcode subroutine comprises performing register name replacements using replacement register names stored in a first alias table element *(micro-alias register)* and wherein said dispatching the one or more operation in the second microcode subroutine comprises performing register name replacements using replacement register names stored in a second alias table element *(micro-alias register) (Each generic microcode routine has micro-alias registers that it uses to replace register names within the routine; column 12, lines 36-56)*;

Subsequent to said dispatching, detecting a branch misprediction within the first microcode subroutine *(a mispredicted micro-branch; column 23, lines 12-35)*;

In response to said detecting, replacing register names within one or more other operations included in the first microcode subroutine with replacement register names stored in the first alias table element *(micro-alias register) (When operation flow restarts at the actual micro-branch target, the register names will be replaced with that stored in the micro-alias register; column 23, lines 12-35; column 12, lines 36-56; See Fig. 14, component 1430)*; and

Dispatching the one more other operations subsequent to said replacing (See Fig. 14, component 1440).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 2-6, 18-22, and 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran in view of Carbine et al., U.S. Patent No. 5,630,083 (Herein referred to as Carbine).

21. Referring to claim 2, Tran has taught the microprocessor of claim 1.

Tran has not explicitly taught that the dispatch unit is further configured to dispatch an operation that provides one or more register names for use as replacement register names within the microcode subroutine.

Carbine has taught a dispatch unit *(MS unit; Fig. 5, component 534)* that is configured to dispatch an operation *(LOADUAR signal)* that provides one or more register names for use as replacement register names within the microcode subroutine *[Carbine; column 12, lines 24-67].*

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the dispatch unit of Tran to dispatch an operation that

provides one or more register names for use as replacement register names with the microcode subroutine as taught by Carbine.

The suggestion/motivation for doing so would have been that a generic microcode routine can be used by any number of other microcode programs *(Carbine; column 12, lines 49-52)*.

Therefore, it would have been obvious to combine Carbine with Tran to obtain the invention as specified in claim 2.

22. Referring to claim 3, Tran and Carbine have taught the microprocessor of claim 2, wherein the dispatch unit is configured to allocate an alias table element *(Carbine; micro-alias register; Fig. 5, component 562)* to store the one or more register names in response to handling the operation *(Carbine; column 12, lines 15-35)*.

23. Referring to claim 4, Tran and Carbine have taught the microprocessor of claim 2, wherein the dispatch unit is configured to maintain multiple allocated alias table elements *(Carbine; micro-alias registers; Fig. 5, component 562)* at a same time *(Carbine; column 12, lines 15-35)*.

24. Referring to claim 5, Tran and Carbine have taught the microprocessor of claim 4, wherein each of the multiple allocated alias table elements (micro-alias registers) is associated with a respective microcode subroutine *(Carbine; The generic microcode routine that uses that particular allocated micro-alias register; See column 12, lines 49-56)*, wherein the dispatch unit is configured to maintain each alias table element at least until all branch operations within the respective microcode subroutine have resolved *[Carbine; If a micro-branch (a branch in microcode) is mispredicted the dispatch unit*

updates/maintains the micro-alias registers so that execution can restart at the actual target of the micro-branch. Therefore, the dispatch unit maintains each micro-alias register until all branch operations within the respective microcode subroutine have resolved; See column 23, lines 12-35].

25. Referring to claim 6, Tran and Carbine have taught the microprocessor of claim 4, wherein in response to detection of a branch misprediction with a microcode subroutine, the dispatch unit is configured to perform replacements within one or more microcode operations included within the microcode subroutine according to the one or more register names stored within a respective alias table element and to dispatch the one more microcode operations subsequent to performing the replacements *(Carbine; column 23, lines 12-35)*.

26. Referring to claim 18, given the similarities between claim 2 and claim 18 the arguments as stated for the rejection of claim 2 also apply to claim 18.

27. Referring to claim 19, given the similarities between claim 3 and claim 19 the arguments as stated for the rejection of claim 3 also apply to claim 19.

28. Referring to claim 20, given the similarities between claim 4 and claim 20 the arguments as stated for the rejection of claim 4 also apply to claim 20.

29. Referring to claim 21, given the similarities between claim 5 and claim 21 the arguments as stated for the rejection of claim 5 also apply to claim 21.

30. Referring to claim 22, given the similarities between claim 6 and claim 22 the arguments as stated for the rejection of claim 6 also apply to claim 22.

31. Referring to claim 30, given the similarities between claim 2 and claim 30 the arguments as stated for the rejection of claim 2 also apply to claim 30.

32. Referring to claim 31, given the similarities between claim 3 and claim 31 the arguments as stated for the rejection of claim 3 also apply to claim 31.

33. Referring to claim 32, given the similarities between claim 6 and claim 32 the arguments as stated for the rejection of claim 6 also apply to claim 32.

34. Referring to claim 33, given the similarities between claim 5 and claim 33 the arguments as stated for the rejection of claim 5 also apply to claim 33.

35. Referring to claim 34, given the similarities between claim 5 and claim 34 the arguments as stated for the rejection of claim 5 also apply to claim 34.

36. Claims 7-8, 23-24, and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran and Carbine as applied to claim 2 above, and further in view of Rotenberg et al., "Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching" (Herein referred to as Rotenberg).

37. Referring to claim 7, Tran and Carbine have taught the microprocessor of claim 2 wherein the dynamic instruction stream includes a microcode subroutine call operation *(Tran; column 8, line 55 – column 9, line 4)* and the one or more register names for use as replacement register names (*Carbine; part of the LOADUAR instruction - column 12, lines 24-67)*.

Tran and Carbine have not explicitly taught a trace cache coupled to the dispatch unit, wherein the trace cache includes a trace cache entry; wherein a trace stored in the trace cache entry includes instructions from the dynamic instruction stream.

Rotenberg has taught a trace cache coupled to the dispatch unit, wherein the trace cache includes a trace cache entry *(Rotenberg; See Section 1.1 and Fig. 2)*. Rotenberg has further taught that a trace stored in the trace cache entry includes instructions from the dynamic instruction stream *(Rotenberg; See Section 1.1)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the system of Tran and Carbine to include a trace cache coupled to the dispatch unit, wherein the trace cache includes a trace cache entry; wherein a trace stored in the trace cache entry includes instructions from the dynamic instruction stream as taught by Rotenberg.

The suggestion/motivation for doing so would have been that the trace cache improves the performance of the microprocessor *(Rotenberg; See Abstract)*.

Therefore, it would have been obvious to combine Rotenberg with Tran and Carbine to obtain the invention as specified in claim 7.

38. Referring to claim 8, Tran, Carbine, and Rotenberg have taught the microprocessor of claim 7, wherein in response to receiving the trace from the trace cache, the dispatch unit is configured to allocate an alias table *(Carbine; micro-alias register; Fig. 5, component 562)* to store the one or more register names *(In response to receiving the LOADUAR instruction, a micro-alias register is allocated - Carbine; column 12, lines 15-35)*.

39. Referring to claim 23, given the similarities between claim 7 and claim 23 the arguments as stated for the rejection of claim 7 also apply to claim 23.

40. Referring to claim 24, given the similarities between claim 8 and claim 24 the arguments as stated for the rejection of claim 8 also apply to claim 24.

41. Referring to claim 35, given the similarities between claim 7 and claim 35 the arguments as stated for the rejection of claim 7 also apply to claim 35.

42. Referring to claim 36, given the similarities between claim 8 and claim 36 the arguments as stated for the rejection of claim 8 also apply to claim 36.

43. Claims 9, 10, 25, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran in view of Kling, U.S. Patent Publication No. 2004/0049657.

44. Referring to claim 9, Tran has taught the microprocessor of claim 1.

Tran has not explicitly taught that the dispatch unit is configured to store the microcode subroutine in one or more microcode traces.

Kling has taught a dispatch unit *(Kling; microcode unit; Fig. 2, component 46; paragraph 13)* that is configured to store a microcode subroutine in one or more microcode traces *(Kling; paragraph 32 on page 4)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the dispatch unit of Tran to be configured to store the microcode subroutine in one or more microcode traces as taught by Kling.

The suggestion/motivation for doing so would have been that the microcode traces enable more efficient processing of the instructions included in the trace upon subsequent invocations *(Kling; paragraph 32 on page 4)*.

Therefore, it would have been obvious to combine Kling with Tran to obtain the invention as specified in claim 9.

45. Referring to claim 10, Tran and King have taught the microprocessor of claim 9, wherein the one or more microcode traces are stored within a memory *(Kling; trace cache; paragraph 32 on page 4)*.

46. Referring to claim 25, given the similarities between claim 9 and claim 25 the arguments as stated for the rejection of claim 9 also apply to claim 25.

47. Referring to claim 37, given the similarities between claim 9 and claim 37 the arguments as stated for the rejection of claim 9 also apply to claim 37.

48. Claims 11-14, 26, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran and Kling as applied to claim 9 above, and further in view of Harris, U.S. Patent No. 6,260,138.

49. Referring to claim 11, Tran and Kling have taught the microprocessor of claim 9, wherein microcode operations are stored in one or more microcode traces *(see claim 9)*.

Tran and Kling have not explicitly taught that each operation includes an associated liveness indication.

Harris has taught an instruction cache wherein each operation includes an associated liveness indication *(Harris; priority tag; column 3, lines 28-31).*

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the trace of Tran and Kling to include an associated liveness indication *(priority tag)* with each operation as taught by Harris.

The suggestion/motivation for doing so would have been that priority tags provide "enhanced performance with respect to conventional predictive branching without the additional cost of duplicated hardware as required by multiway branching *(Harris; column 10, lines 20-24).*

Therefore, it would have been obvious to combine Harris with Tran and Kling to obtain the invention as specified in claim 11.

50. Referring to claim 12, Tran, Kling, and Harris have taught the microprocessor of claim 11, wherein the dispatch unit *(Harris; dispatch unit; Fig. 8, component 26)* is configured to determine whether each microcode operation stored in one of the one or more microcode traces is executable *(i.e. on the predicted path)* dependent on at least one of: a branch prediction and the associated liveness indication *(priority tag) (Harris; column 5, lines 27-34)*;

wherein the dispatch unit is configured to signal whether each microcode operation stored in the one of the one or more microcode traces is executable when dispatching that microcode operation to the scheduler *(Harris; execution buffer; Fig. 8, component 126) [Harris; The dispatch unit signals whether each operation is*

executable by sending the priority tag to the scheduler (execution buffer); column 9, lines 38-39];

wherein the scheduler *(execution buffer)* is configured to store an associated indication *(priority tag)* for each dispatched microcode operation indicating whether that dispatched microcode operation is executable *(Harris; column 9, lines 38-46)*.

51. Referring to claim 13, Tran, Kling, and Harris have taught the microprocessor of claim 12, wherein if the branch predication is incorrect, the scheduler is configured to update the associated indication for at least one dispatched microcode operation *(Harris; column 8, lines 6-39)*.

52. Referring to claim 14, Tran, Kling, and Harris have taught the microprocessor of claim 11, wherein the dispatch unit is configured to selectively dispatch microcode operations included in the one or more microcode traces dependent upon at least one of: the associated liveness indication (priority tag) and branch prediction *(Harris; The dispatch unit selects instruction for dispatch from those having the highest priority (as indicated by the priority tag) to those having the lowest - column 7, lines 44-51)*.

53. Referring to claim 26, given the similarities between claim 11 and claim 26 the arguments as stated for the rejection of claim 11 also apply to claim 26.

54. Referring to claim 38, given the similarities between claim 11 and claim 38 the arguments as stated for the rejection of claim 11 also apply to claim 38.

Response to Arguments

55. Applicants arguments filed on April 27, 2006, have been fully considered but they are not found persuasive.

56. Applicant argues the novelty/rejection of claims 1 and 17 on pages 12-13 of the remarks, in substance that:

> "Tran fails to teach or suggest *a scheduler coupled to the dispatch unit and configured to schedule dispatched operations for execution, wherein in response to receiving a microcoded instruction, the dispatch unit is configured to dispatch to the scheduler a microcode subroutine call operation that includes a tag identifying a microcode subroutine associated with the microcoded instruction*" *(2nd paragraph on page 12)*

These arguments are not found persuasive for the following reasons:

Tran has taught executing instructions that invoke microcode subroutines (i.e. microcoded instructions). Tran has further taught using the x86 CALL instruction as a microcoded instruction *[Tran; column 4, lines 42-65]*. The execution of the x86 CALL instruction involves the storing of context information (such as the instruction pointer) in addition to the execution of the microcode subroutine instructions *[See definition of x86 CALL instruction on page 4-5 in Manual]*. In order for context information to be stored, the x86 CALL instruction itself must be executed by one of the execution units of the processor. Execution by one of the execution units requires that the instruction be dispatched from decode unit (part of the dispatch unit) to the reservation station (i.e. the scheduler) associated with the desired execution unit. It is this act of dispatching the x86 CALL instruction from the decode unit to the reservation station that reads upon the claim limitation "wherein in response to the receiving a microcoded instruction, the dispatch unit is configured to dispatch to the

scheduler a microcode subroutine call operation". Therefore, it is not the act of sending an instruction indication from the decode unit to the microcode unit that is interpreted as reading upon the above-quoted limitation as argued by the Applicant.

57. Applicant argues the novelty/rejection of claims 29 and 41 on pages 13-15 of the remarks, in substance that:

> "Tran fails to teach or suggest detecting a microcoded instruction within the stream of instructions, wherein the microcoded instruction immediately precedes an other instruction in program order, in response to said detecting, dispatching a microcode subroutine call operation that identifies a microcode subroutine associated with the microcoded instruction" *(4th full paragraph on page 13)*

> Examiner's citation "has nothing to do with pushing or popping an instruction onto or off of a stack as part of a microcode subroutine call operation dispatched in response to detecting a microcoded instruction" *(2nd full paragraph on page 14)*

These arguments are not found persuasive for the following reasons:

Tran has taught detecting within an instruction stream an "instruction to be performed by the microcode unit" (i.e. a microcoded instruction) *[Tran; column 4, lines 36-41]*. Tran has further taught that the decode unit fetches and dispatches instructions once again after the microcode unit has completed dispatching the routine associated with the microcoded instruction *[Tran; column 4, lines 36-41]*. Therefore, there are instructions in program order immediately following the microcoded instruction. That is, the microcoded instruction immediately precedes instructions in program order.

In response to Applicant's argument regarding the claim limitation "dispatching a microcode subroutine call operation", the Examiner refers Applicant to the remarks made above in response to the arguments for claim 1.

Tran has taught that a subroutine call instruction, which is dispatched in response to detecting a microcoded instruction, "stores the address of the following instruction within a predefined storage location" *[Tran; column 4, lines 42-47]*. Tran has further taught that the subroutine, which is dispatched in response to detecting a microcoded instruction, includes a subroutine return instruction that "causes instruction execution to continue at the address stored by the subroutine call instruction" *[Tran; column 4, lines 47-52]*. When using the x86 CALL and RETURN instructions as taught by Tran *[Tran; column 4, lines 52-54]*, the storing and reading of the instruction address following the microcoded instruction to a predefined location consists of push and pop operations to and from the stack *[See definition of x86 CALL and RETURN instructions on page 4-5 in Manual]*. Therefore, Tran teaches a microcode subroutine call operation that pushes an address of the other instruction onto a stack, that the microcode subroutine includes a return operation, and that execution of the return operation pops the address from the stack.

In response to Applicant's argument that the CALL instruction is not a microcoded instruction, the Examiner notes that the CALL instruction is a microcoded instruction as the operation to be executed in response to the instruction is, at least partially, contained within microcode *[Tran; column 4, lines 36-54]*. That is, the CALL instruction invokes microcode. As noted above, in response to detecting the CALL instruction the CALL instruction is dispatched. This dispatched CALL instruction is a microcode subroutine call operation. Therefore, the CALL instruction is both a microcoded instruction and microcode subroutine call operation.

58. Applicant argues the novelty/rejection of claim 40 on pages 15-16 of the remarks, in substance that:

> "Carbine fails to teach or suggest *dispatching one or more operations included in a first microcode subroutine and one or more operations included in a second microcode subroutine, wherein said dispatching the one or more operations in the first microcode subroutine comprises performing register name replacements using replacement register names stored in a first alias table element and wherein said dispatching the one or more operations in the second microcode subroutine comprises performing register name replacements using replacement register names stored in a second alias table element*" *(3rd full paragraph on page 15)*

These arguments are not found persuasive for the following reasons:

In response to Applicant's argument that Carbine has only taught a single micro-alias register (i.e. alias table element), the Examiner notes that Carbine specifically refers to a plurality of micro-alias registers at column 12, lines 36-39.

In response to Applicant's argument that Carbine has only taught dispatching single generic microcode routine (i.e. microcode subroutine), the Examiner notes that while Carbine refers to a single generic rounding microcode routine as an example of a generic microcode routine, Carbine also states that "the registers are not hard-coded into any routine" *[Carbine; column 12, lines 52-56],* thereby indicating multiple generic microcode routines are used. Therefore, Carbine has taught dispatching multiple generic microcode routines.

Conclusion

59. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

60. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

61. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chen, U.S. Patent No. 6,356,995, teaches a processor that detects microcoded instructions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

Fritz M. Fleming

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

7/7/2006